**CMOS design for FPGA matrix.**

**ABSTRACT**

FPGA has been proposed as a way of obtaining high performance for computationally intensive DSP applications such as image processing (IP), even under real time requirements. The inherent reprogrammability of FPGAs gives them some of the flexibility of software while keeping the performance advantages of an (ASIC) application specific solution. However, a major disadvantage of FPGAs is their low level programming model. To bridge the gap between these two levels, the authors present a high level software environment for FPGA-based image processing, which aims to hide hardware details as much as possible from the user. Their approach is to provide a very high level image processing coprocessor (IPC) with a core instruction set based on the operations of image algebra.

The environment includes a generator which generates optimised architectures for specific user-defined operations. The entire stereo vision process, such as rectification, stereo matching, and post-processing, is realized using a single field programmable gate array (FPGA) without the necessity of any external devices. The hardware implementation is more than 230 times faster when compared to a software program operating on a conventional computer, and shows stronger performance over previous hardware-related studies. Dynamic reconfiguration of field programmable gate arrays (FPGAs) has recently emerged as the next step in reconfigurable computing. The device being developed is capable of storing four configurations on-chip and switching between them on a clock cycle basis. Configurations can be loaded while other contexts are active. A powerful cross-context data sharing mechanism has been implemented. The current status of this work and future work are described. we show that our proposed architectureis scalable by presenting the results for 6 x 6 and 8 x 8 matrices.

**HDLUSED:**

Verilog

**TOOLS:**

* Dsch (Digital schematic).
* Microwind.